Claims:

1. **Bi-stable latch circuit** having a pair of cross-coupled branches (I,II), each branch including a complementary driver and a load connected between a drain line and a source line and a non-volatile memory cell having a program transistor and a read transistor,
   - at least one of said drivers and loads including said read transistor,
   - said driver and load of said branch connected in series at a respective output node,
   - said read transistor and program transistor having a common floating gate and separate control gates,
   - said control gate of said program transistor connected to a program voltage,
   - the drain of said program transistor connected to a respective input node,
   - said control gate of said read transistor in said branch connected to said output node of the other branch (II).

2. Latch circuit according to claim 1, wherein at least one of said read transistor or program transistor is a semiconductor device using hot electron injection for changing a threshold voltage thereof.

3. Latch circuit according to claim 1 or claim 2, wherein said drain and source line are connected across a common supply voltage in static mode but at least one of said drain and source line is disconnected from said common supply voltage in a program mode.

4. Latch circuit or **Method for its** programming, preferably according to any one of the preceding claims, wherein said inputs are held at logic low level in said static mode but the voltage at one of said inputs is raised to a voltage high enough to generate hot electrons or hot holes at the drain of a respective program transistor in a program mode.

5. Latch circuit or Method according to any one of the preceding claims, wherein said program voltage is connected to said supply voltage in said static mode but said program voltage is raised to a voltage high enough to attract electrons or holes into said floating gate in said program mode.

6. Latch circuit substantially as described with reference to the accompanying drawings.

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